SYSTEM AND METHOD FOR SITE-TO-SITE YIELD COMPARISON WHILE TESTING INTEGRATED CIRCUIT DIES

ABSTRACT OF THE DISCLOSURE

Disclosed herein are systems and methods for testing the functionality of a plurality of integrated circuit dies formed in a plurality of rows on a semiconductor wafer. In one embodiment, the system includes a probe device having at least two probing areas configured to test the functionality of the plurality of dies. The first probing area of the at least two probing areas is positioned to test each of a plurality of dies in a first row of the plurality of rows and a second probing area of the at least two probing areas is positioned to test each of a plurality of dies in a second row of the plurality of rows simultaneously with the first probing area. The system also includes a tester device coupled to the probe device and configured to compare test data received from the die in the first row with test data received from the die in the second row.